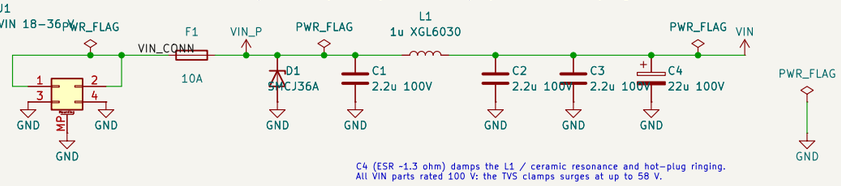
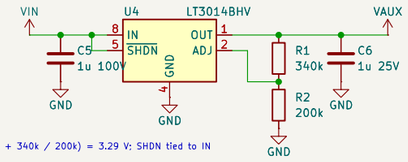
INPUT 18–36 V: fuse + TVS crowbar (reverse polarity blows F1), pi filter, damping



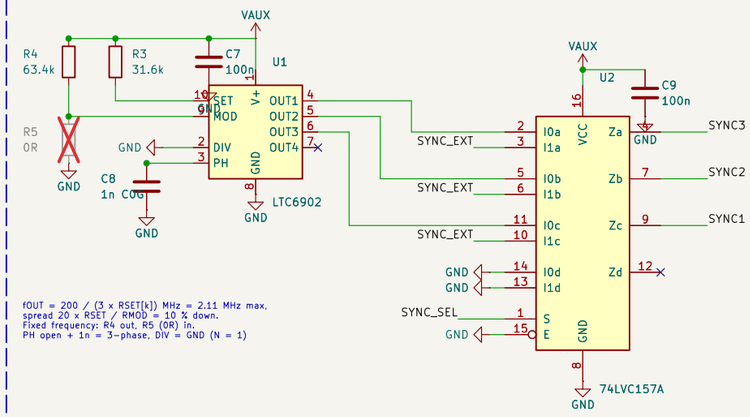
C4 (ESR ~1.3 ohm) damps the L1 / ceramic resonance and hot-plug ringing.
All VIN parts rated 100 V: the TVS clamps surges at up to 58 V.

AUX 3.3 V (always on): LT3014BHV 80 V, 20 mA



VOUT = 1.22 V x (1 + 340k / 200k) = 3.29 V; SHDN tied to IN

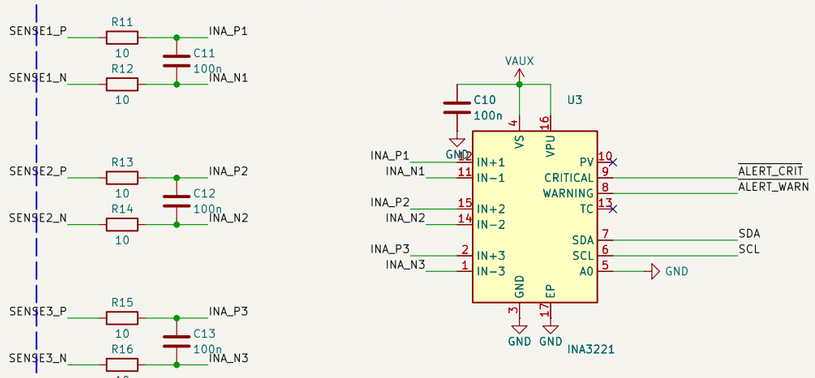
CLOCK: LTC6902 3-phase 2.11 MHz, 10 % down-spread; 74LVC157A source select



fOUT = 200 / (3 x RSET[k]) MHz = 2.11 MHz max, spread 20 x RSET / RMOD = 10 % down.
Fixed frequency: R4 out, R5 (0R) in.
PH open + 1n = 3-phase, DIV = GND (N = 1)

SYNC_SEL low (default, 100k pull-down) = LTC6902 3-phase; high = SYNC_IN to all three in phase.
No clock: SYNC low = Burst Mode (fallback)

MONITOR: INA3221 at I2C 0x40 (A0 = GND); CH1 = 12 V, CH2 = 5 V, CH3 = 3.3 V



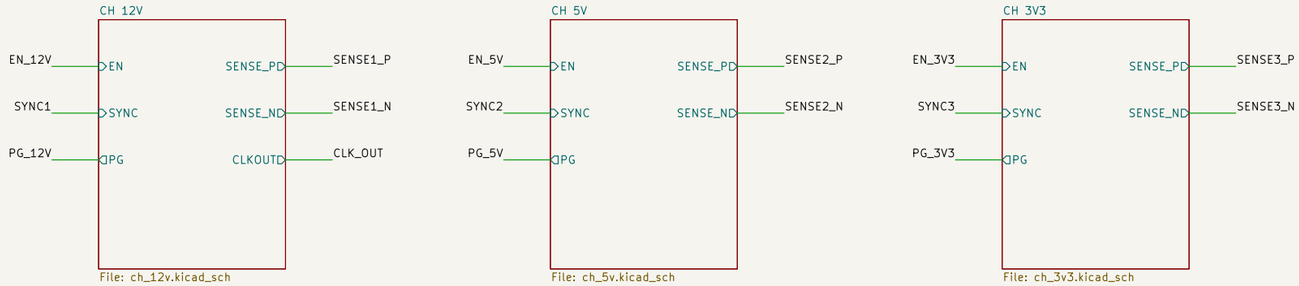
10 ohm + 100n differential at the INA3221 (data sheet 7.4.3)

PV and TC unused (PV defaults to 9 / 10 V limits).
Alerts are open drain, active low.

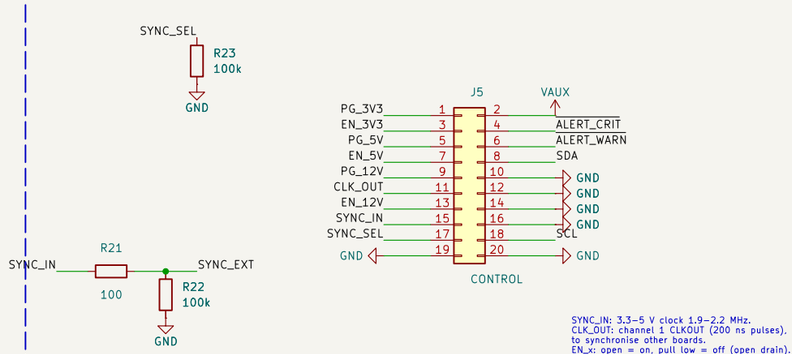
PULL-UPS to VAUX: I2C 4.7k (JP1 bridged; cut to remove), alerts 10k



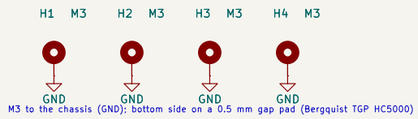
CHANNELS (one sheet each)



CONTROL: Samtec SHF-110 2 x 10, 1.27 mm (ribbon FFSD-10-D)



SYNC_IN: 3.3–5 V clock 1.9–2.2 MHz.
CLK_OUT: channel 1 CLKOUT (200 ns pulses), to synchronise other boards.
EN_x: open = on, pull low = off (open drain).
PG_x: open drain to VAUX (100k)



M3 to the chassis (GND); bottom side on a 0.5 mm gap pad (Bergquist TGP HC5000)

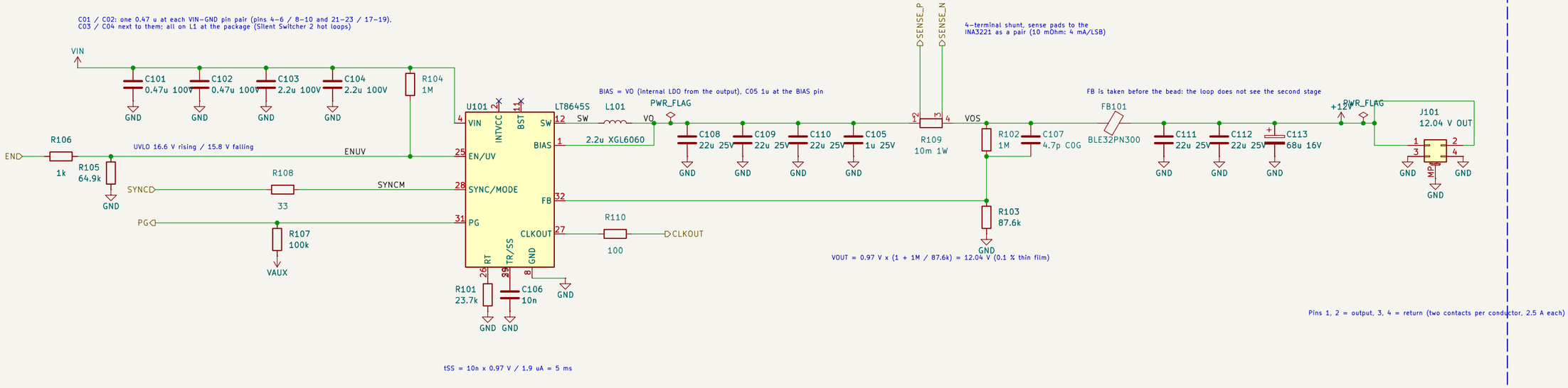
6 layers JLC061621-3313, parts on top, bottom on a chassis thermal pad
INA3221 I2C monitor, EN / PG per channel, fuse + TVS, pi / bead filters
3 x LT8645S Silent Switcher 2, 2 MHz, 3-phase sync or external clock

Sheet: /
File: triple_buck.kicad_sch

Title: Triple synchronous buck 18–36 V to 12 V / 5 V / 3.3 V, 5 A each

Size: A3	Date: 2026-11-02	**Rev: 3**
KiCad E.D.A. 10.0.4		Id: 1/4

CHANNEL 12V: LT8645S, 12.04 V / 5 A, 2 MHz class (sync), RT 23.7k = 1.6 MHz free-running



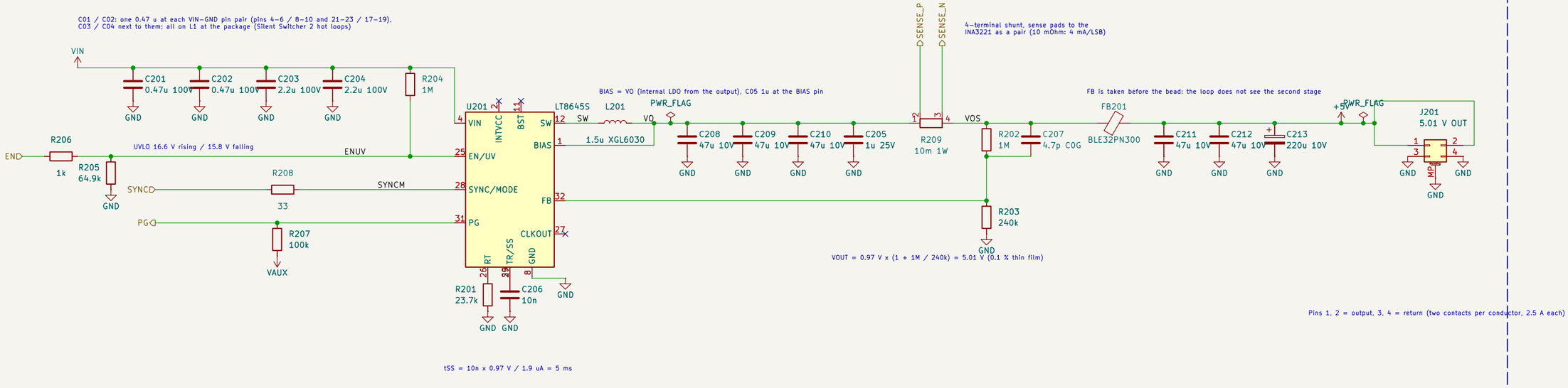
6 layers JLC061621-3313, parts on top, bottom on a chassis thermal pad
INA3221 I2C monitor, EN / PG per channel, fuse + TVS, pi / bead filters
3 x LT8645S Silent Switcher 2, 2 MHz, 3-phase sync or external clock

Sheet: /CH 12V/
File: ch_12v.kicad_sch

Title: Channel 12V

Size: A3	Date: 2026-11-02	**Rev: 3**
KiCad E.D.A. 10.0.4		Id: 2/4

CHANNEL 5V: LT8645S, 5.01 V / 5 A, 2 MHz class (sync), RT 23.7k = 1.6 MHz free-running



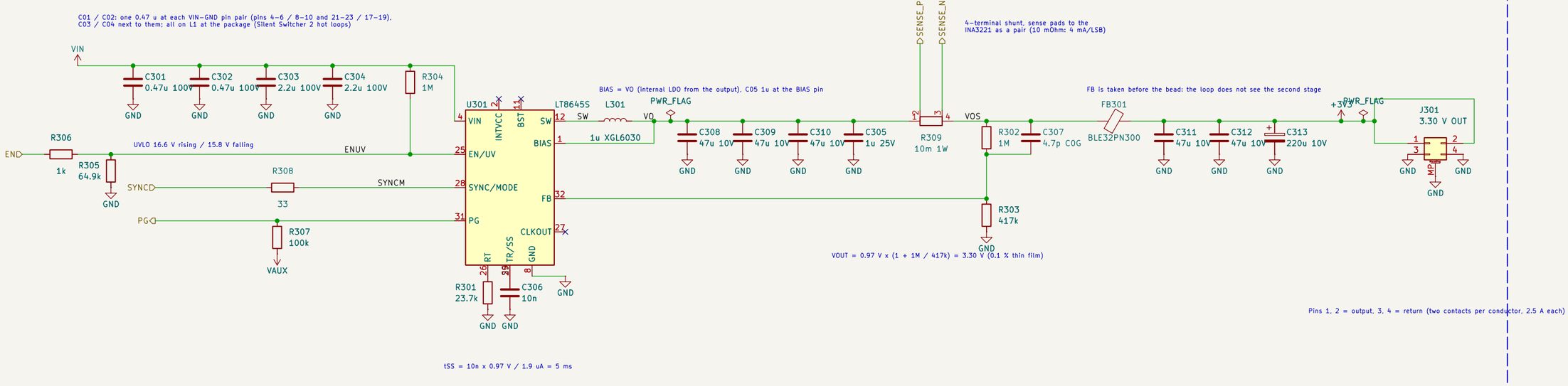
6 layers JLC061621-3313, parts on top, bottom on a chassis thermal pad
INA3221 I2C monitor, EN / PG per channel, fuse + TVS, pi / bead filters
3 x LT8645S Silent Switcher 2, 2 MHz, 3-phase sync or external clock

Sheet: /CH 5V/
File: ch_5v.kicad_sch

Title: Channel 5V

Size: A3	Date: 2026-11-02	**Rev: 3**
KiCad E.D.A. 10.0.4		Id: 3/4

CHANNEL 3V3: LT8645S, 3.30 V / 5 A, 2 MHz class (sync), RT 23.7k = 1.6 MHz free-running



6 layers JLC061621-3313, parts on top, bottom on a chassis thermal pad
INA3221 I2C monitor, EN / PG per channel, fuse + TVS, pi / bead filters
3 x LT8645S Silent Switcher 2, 2 MHz, 3-phase sync or external clock

Sheet: /CH 3V3/
File: ch_3v3.kicad_sch

Title: Channel 3V3

Size: A3	Date: 2026-11-02	**Rev: 3**
KiCad E.D.A. 10.0.4		Id: 4/4